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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/618,955	07/14/2003	Chae Kyu Jang	CU-3290 RJS	6419
26530	7590	10/21/2005	EXAMINER	
LADAS & PARRY LLP 224 SOUTH MICHIGAN AVENUE SUITE 1600 CHICAGO, IL 60604			PAREKH, NITIN	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 10/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/618,955

Applicant(s)

JANG ET AL.

Examiner

Nitin Parekh

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 16 August 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1, 2, 5 and 6 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1, 2 and 6 is/are rejected.
- 7) ☒ Claim(s) 5 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Claim Objections***

1. Claim 5 depends on claim 4, which is cancelled. Accordingly, claim 5 should be cancelled.

### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 2, 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinsman (US Pat. Application Pub. 2002/0038442) in view of Ochi et al. (US Pat. 5416358) and the admitted prior art (APA).

Regarding claims 1, 2, 4 and 6, Kinsman disclose a ball grid array (BGA) package comprising:

- a printed circuit board (PCB- 2 in Fig. 9) having bonding sites/fingers/pads
- an adhesive material (not numerically referenced in Fig. 9) being coated on the edges of the PCB (50/54 in section 0031)
- a sealing frame having a plurality of sealing posts comprising vertical sidewalls located at each peripheral sides (see 12 and 26 respectively in Fig. 9) made of a

barrier material including an insulating/non-conductive material (see sections 0030/0031) being adhered on the adhesive material/PCB, the SF/SP including a recess/lip at an upper end of the vertical wall (see 66 in Fig. 9; section 0034)

- a plurality of semiconductor chips including a single chip having a plurality of bonding pads (52/56 in Fig. 8/9) adhered on the PCB, the chips being the edge-pad type chip
- a plurality of aluminum/metal wires (60 in Fig. 9) separately connecting bonding pads of the chip to the bonding sites/fingers of the PCB
- a sealing cover/cap (SC-62 in Fig. 9) made of an insulating/non-conductive material such as glass/quartz (see section 0032) being adhered on the recessed portion of the SF/SP, the SC sealing the semiconductor chip
- the SC being adhered on the recessed portion of the sealing posts using conventional adhesive material including an adhesive tape/low temperature thermoplastic tape (see sections 0031-0034), the SC being connected to the vertical walls of the sealing posts for sealing the chips/single chip from the top and the sealing posts enclose the lateral sides of the chips/single chip, and
- a plurality of conductive elements/solder balls (see 74 in Fig. 13; section 0036) adhered to a lower side of the PCB

(Fig. 9; Fig. 8 and 13; sections 30-36 and 24-29).

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Kinsman fails to teach:

a) an extrusion connected to an upper end of the vertical wall of the each sealing post and the SC being adhered to one or more extrusions wherein the extrusions are inside the enclosure

b) the package being a test vehicle comprising a testing chip.

a) Ochi et al. teach a PCB package having a sealing frame/post (see 7/7a/7b in Fig. 13/14) wherein each sealing post comprises a vertical wall (7 in Fig. 13/14), the wall having a plurality of extruded portions/extrusions (see projected portion above rib 7a and the rib 7a in Fig. 13/14) connected to an upper/middle portion of the wall, the extrusions being inside the enclosure (Col. 10, lines 2-62). The PCB package further comprises a sealing/cover plate being adhered to the extrusions through an adhesive film and a sealing resin (see 5a and 6a/9/10 in Fig. 14).

Furthermore, parameters including size/dimension/thickness of components such as frame, substrate, cover plate, etc., location/positioning of the recess/extrusion, spacing of the above from the bonding pad/wire, etc. in chip packaging and interconnect technology is a subject of routine experimentation and optimization to achieve the desired package dimensions/weight, rigidity/strength and reliability.

b) The APA teaches using conventional packages in a form of a test vehicle package to test semiconductor chips (see specification pages 1–3).

It would have been obvious to a person of ordinary skill in the art at the time invention was to incorporate elements a) and b) as taught by Ochi et al. and APA so that the rigidity/strength for the sealing post/frame and the package can be improved and testing/characterization capability can be enhanced in Kinsman's BGA.

### ***Response to Arguments***

3. Applicant's arguments with respect to claims 1, 2 and 6 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's acting supervisor, Steven Loke can be reached on 571-272-1657.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAN or Public PAG. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAG system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Any inquiry of a general nature or relating to the

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status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

NP

09-17-05



NITIN PAREKH

PRIMARY EXAMINER  
TECHNOLOGY CENTER 2800